IN THE CLAIMS

Please amend the claims as follows:

1. (Canceled)

2. (Currently Amended) A method for forming a semiconductor device, comprising:

forming an insulation layer in a capacitor region and a metal interconnection region on a substrate;

forming a first trench in the insulation layer of ~~at~~ the capacitor region and the metal interconnection region ~~of the insulation layer~~;

forming ~~the~~ a first metal interconnection inside the first trench;

forming a second trench by ~~removing~~ selectively etching the insulation layer in the capacitor region between the first metal interconnection;

forming a capacitor in the second trench; and

forming a second metal interconnection over the first metal interconnection,

wherein the capacitor and the first metal interconnection are ~~is~~ formed in a substantially equivalent vertical plane~~the same layer~~ of the semiconductor device ~~with the first metal interconnection~~.

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3. (Currently Amended) A method for forming a semiconductor device, comprising:

forming an insulation layer in a capacitor region and a metal interconnection region on a substrate;

forming a first trench in the insulation layer of the capacitor region and the metal interconnection region ~~of the insulation layer~~;

forming a first barrier metal and ~~the~~ a first metal interconnection inside the first trench;

forming a second trench by ~~removing~~ selectively etching the insulation layer in the capacitor region around the first barrier metal;

forming a third trench in the first barrier metal by selectively etching ~~removing~~ the first metal interconnection in the capacitor region; ~~and~~

forming a capacitor in the second and the third trenches; and

forming a second metal interconnection over the first metal interconnection,

wherein the capacitor and the first metal interconnection are ~~is~~ formed in a substantially equivalent vertical plane of the semiconductor device ~~in the same layer with the first metal interconnection~~.

4. (Canceled)

5. (Currently Amended) The method as recited in claim 2, wherein the first metal interconnection ~~is of~~ includes copper.

6. (Currently Amended) The method as recited in claim 2, wherein the capacitor includes first and ~~the~~ second electrodes ~~are~~ formed of a metal selected from a group of Pt, Ru, Ir and W.

7. (Currently Amended) The method as recited in claim 2, wherein the capacitor includes a dielectric layer ~~is~~ formed of an oxide selected from a group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.

8. (Currently Amended) A method for fabricating a semiconductor device, comprising:

forming ~~an insulation layer including~~ a first insulation layer ~~and a second insulation layers~~ in ~~the~~ a capacitor region and ~~the~~ a metal interconnection region on a substrate formed with a lower conductive layer;

forming a second insulation layer on the first insulation layer;

forming an interconnection trench in the metal interconnection region~~,~~ and a first trench in the capacitor region by selectively etching the second insulation layer;~~,~~

forming~~, and~~ a via hole connected to the lower conductive layer by selectively etching the first insulation layer;

forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench;

forming a second trench by selectively etching the second insulation layer of the capacitor region;

forming a capacitor in the second trench; and

forming a barrier layer on the capacitor and a second copper ~~interconnection~~ layer on the barrier layer.

9. (Currently Amended) The method as recited in claim 8, further comprising forming ~~wherein the insulation layer includes~~ an etching blocking layer between the first insulation layer and the second insulation layer.

10. (Currently Amended) The method as recited in claim 8, further comprising forming ~~including~~ a hard mask on the second insulation layer.

11. (Previously Presented) The method as recited in claim 8, wherein forming the interconnection trench further comprises forming the interconnection trench and the first trench simultaneously prior to forming the via hole.

12. (Currently Amended) The method as recited in claim 8, wherein forming the interconnection trench further comprises forming the via hole first by selectively etching the first and second insulation layers, and then forming the interconnection trench and the first trench simultaneously.

13. (Currently Amended) The method as recited in claim 8, wherein the first and the second copper ~~conductive~~ layers are formed using ~~use~~ a reflow method after ~~forming a layer~~ disposing copper in a sputtering method, a CVD method or an electroplating method.

14. (Currently Amended) The method as recited in claim ~~8~~ 13, ~~wherein in case of using~~ the electroplating method further comprises, forming a seed layer ~~is formed in a~~ by

method selected from ~~a~~ the group consisting of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) and an electroless deposition, or a combination thereof.

15. (Previously presented) The method as recited in claim 8, further including forming a first barrier metal prior to the first copper layer.

16. (Currently Amended) A method for fabricating a semiconductor device, comprising:

forming an insulation layer in the metal interconnection region and the capacitor region on ~~the~~ a substrate formed with a lower conductive layer;

forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer;

forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench;

forming a second trench by selectively etching the ~~second~~ insulation layer around the first copper interconnection in the capacitor region;

forming a third trench in the first barrier metal by selectively etching the first copper interconnection;

forming a capacitor in the second and the third trenches; and

forming a second copper interconnection by forming a second copper layer on the capacitor.

17. (Original) The method as recited in claim 16, wherein a second barrier metal is formed prior to the formation of the second copper layer.

18. (Currently Amended) The method as recited in claim ~~16~~ 17, wherein the first and the second barrier metals ~~is of~~ includes a metal ~~one~~ selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN, and a combination thereof.

19. (Currently Amended) The method as recited in claim 3, wherein the first metal interconnection ~~is of~~ includes copper.

20. (Currently Amended) The method as recited in claim 3, wherein the capacitor includes first and ~~the~~ second electrodes ~~are~~ formed of a metal selected from a group of Pt, Ru, Ir and W.

21. (Currently Amended) The method as recited in claim 3, wherein the capacitor includes a dielectric layer is of an oxide selected from a group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.